LISTING OF THE CLAIMS

Please amend claim 33; and

Please add new claims 45 and 46 as follows.

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-13. (Canceled)

14. (Previously Presented) A semiconductor device, comprising:

a substrate;

a source and a drain arranged within the substrate;

a gate formed on the substrate between the source and drain; and

a substrate contact formed within the substrate in electrical contact with the source, the substrate contact being arranged adjacent to a side of the source without an intervening shallow trench isolation structure,

wherein little or no current flows through the substrate contact.

15. (Original) The semiconductor device of claim 14, further comprising the substrate contact being configured to shield the semiconductor device from electrical noise.

16. (Original) The semiconductor device of claim 14, further comprising the substrate contact being in direct physical contact with the source of the semiconductor device.

17. (Original) The semiconductor device of claim 14, wherein the substrate contact comprises a p+ region.

18. (Original) The semiconductor device of claim 14, wherein the source comprises a source finger and the substrate contact abuts substantially all of one side of the source finger.

19. (Previously Presented) The semiconductor device of claim 14, wherein the source comprises at least two source fingers arranged within the substrate, wherein the substrate contact abuts two of the at least two source fingers.

20. (Original) The semiconductor device of claim 14, wherein the substrate contact comprises a p-type doped silicon tab contacting the source and a silicide layer arranged on top of the substrate contact.

Claims 21-30. (canceled)

31. (Previously Presented) The semiconductor device of claim 14, wherein the substrate contact at least one of:

completely encircles an active region;

almost completely encircles an active region;

encircles three-quarters of an active region; and

encircles half of an active region.

32. (Previously Presented) The semiconductor device of claim 14, wherein the semiconductor device comprises an FET prime cell.

33. (Currently Amended) A semiconductor device, comprising:

a substrate;

a source and a drain arranged within the substrate;

a gate formed on the substrate between the source and the drain; and

a ring substrate contact formed within the substrate in electrical contact with the source,

wherein one of the ring substrate contact abuts a side of the source [[are]] and is arranged adjacent to the side of the source without an intervening shallow trench isolation structure.

34. (Previously Presented) The semiconductor device of claim 33, wherein the ring substrate contact is configured to shield the semiconductor device from electrical noise.

35. (Previously Presented) The semiconductor device of claim 33, wherein the ring substrate contact is in direct physical contact with the source of the semiconductor device.

36. (Previously Presented) The semiconductor device of claim 33, wherein the ring substrate contact comprises a p+ region.

37. (Previously Presented) The semiconductor device of claim 33, wherein the source comprises a source finger and the ring substrate contact abuts substantially all of one side of the source finger.

38. (Previously Presented) The semiconductor device of claim 33, wherein the source comprises at least two source fingers arranged within the substrate, wherein the ring substrate contact abuts two of the at least two source fingers.

39. (Previously Presented) The semiconductor device of claim 33, wherein the ring substrate contact comprises a p-type doped silicon tab contacting the source and further comprising a silicide layer arranged on top of the ring substrate contact.

40. (Previously Presented) The semiconductor device of claim 33, wherein the semiconductor device comprises an FET prime cell.

41. (Previously Presented) The semiconductor device of claim 33, wherein the ring substrate contact at least one of:

completely encircles an active region;

almost completely encircles an active region;

encircles three-quarters of an active region; and

encircles half of an active region.

42. (Previously Presented) A semiconductor device, comprising:

a substrate;

a source and a drain arranged within the substrate;

a gate formed on the substrate between the source and the drain; and

a substrate contact formed within the substrate in electrical contact with the source, the substrate contact at least one of:

completely encircling an active region;

almost completely encircling an active region;

encircling three-quarters of an active region; and

encircling half of an active region,

wherein one of the substrate contact abuts a side of the source and is arranged adjacent to the side of the source without an intervening shallow trench isolation structure.

43. (Previously Presented) The semiconductor device of claim 42, wherein the semiconductor device comprises an FET prime cell.

44. (Previously Presented) The semiconductor device of claim 14, wherein the substrate contact abuts the side of the source.

45. (New) The semiconductor device of claim 14, wherein the source and the substrate are held at a same voltage potential.

46. (New) The semiconductor device of claim 14, wherein the substrate contact is a p+ contact arranged within an active region and wherein silicide provides electrical contact between the source and the active region.